1. A method, comprising:

disposing two rectangular diffusions of P (+) material in an n-well formed in a p-substrate using a complementary metal oxide semiconductor (CMOS) process;

disposing a polycide gate between the two rectangular diffusions of P (+) material;

disposing a pair of inductors on the substrate; and

coupling the two rectangular diffusions of P (+) material and the pair of inductors in a voltage-controlled oscillator (VCO) configuration.

2. The method of claim 1 wherein disposing two rectangular diffusions of P (+) material in an n-well formed in a p-substrate using the CMOS process comprises disposing two rectangular diffusions of P (+) material in an n-well formed in an epitaxial substrate using the CMOS process.

3. The method of claim 1 wherein disposing two rectangular diffusions of P (+) material in an n-well formed in a p-substrate using the CMOS process comprises disposing two rectangular diffusions of P (+) material in an n-well formed in a non-epitaxial substrate using the CMOS process.

4. The method of claim 3 wherein disposing two rectangular diffusions of P (+) material in an n-well formed in a p-substrate using the CMOS process comprises disposing two rectangular diffusions of P (+) material in an n-well diffused in a p-substrate using the CMOS process.

4. The method of claim 3 wherein disposing two rectangular diffusions of P (+) material in an n-well formed in a p-substrate using the CMOS process comprises disposing two rectangular diffusions of P (+) material in an n-well diffused in a p-substrate using the CMOS process.

5. The method of claim 1 wherein disposing two rectangular diffusions of P (+) material in an n-well formed in a p-substrate using the CMOS process comprises building a metal oxide structure on top of the n-well.

6. The method of claim 1 further comprising defining the spacing between the two rectangular diffusions of P (+) material using a lightly doped drain (LDD) structure .

7. The method of claim 1 further comprising defining the spacing between the two rectangular diffusions of P (+) material using halo implantation.

8. A method, comprising:

forming two rectangular diffusions of P (+) material in or on an n-well formed in or on a substrate; and

defining a spacing between the two rectangular diffusions of P (+) material using a polycide gate in a complementary metal oxide semiconductor (CMOS) process.

9. The method of claim 8, further comprising diffusing an n-well into the substrate.

10. The method of claim 9, further comprising diffusing an N (+) well into the n-well.

11. The method of claim 8, further comprising defining a spacing between the two rectangular diffusions of P (+) material using at least one of a lightly doped drain (LDD) structure or halo implantation.

12. The method of claim 8 wherein forming two rectangular diffusions of P (+) material in or on an n-well formed in or on a substrate in a CMOS process comprises forming two rectangular diffusions of P (+) material in or on an n-well formed in or on a non-epitaxial substrate.

13. An apparatus, comprising:

two rectangular diffusions of P (+) material disposed in an n-well diffused into a p-substrate; and

a polycide gate disposed between the two rectangular diffusions of P (+) material in a complementary metal oxide semiconductor (CMOS) process.

14. The apparatus of claim 13 wherein the substrate comprises a non-epitaxial substrate.

15. The apparatus of claim 14, further comprising a lightly doped drain (LDD) disposed between the two rectangular diffusions of P (+) material.

16. The apparatus of claim 14, further comprising a halo implant disposed between the two rectangular diffusions of P (+) material.

17. An article of manufacture, comprising:

machine-readable medium having machine-readable instructions stored thereon to instruct a processor to form two rectangular diffusions of P (+) material in or on an n-well formed in or on a substrate and to define a spacing between the two rectangular diffusions of P (+) material using a polycide gate in a complementary metal oxide semiconductor (CMOS) process.

18. The article of manufacture of claim 17, wherein the machine-readable instructions are further to instruct the processor to diffuse an n-well into the substrate.

19. The article of manufacture of claim 18, wherein the machine-readable instructions are further to instruct the processor to diffuse an N (+) well into the n-well.

20. The article of manufacture of claim 17, wherein the machine-readable instructions are further to instruct the processor to define a spacing between the two rectangular diffusions of P (+) material using at least one of a lightly doped drain (LDD) structure or halo implantation.

21. A system, comprising:

a voltage variable capacitor having two rectangular diffusions of P (+) material disposed in an n-well diffused into a p-substrate and a polycide gate disposed between the two rectangular diffusions of P (+) material in a complementary metal oxide semiconductor (CMOS) process; and

a pair of inductors formed on the substrate in the CMOS process and coupled to the voltage variable capacitor in a voltage-controlled oscillator (VCO) configuration.

24. The system of claim 23, further comprising a charge pump coupled to an output of the phase detector.

25. The system of claim 25 further comprising, a loop filter coupled to an output of the charge pump.

26. The system of claim 25 further comprising a buffer coupled to an output of the loop filter and to the input of the VCO.